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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VO, THANH DUC	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,888	VIHMALO ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-15,17 and 19-35* is/are rejected.

7)☒ Claim(s) *4 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on May 30, 2006. Claims 1-15, and17-35 are presented for examination. Claims 1-15, and 17-35 are pending. All objections or rejections not repeated below have been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-3, 5-15, 19-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US Pub 2004/0177212) in view of Ban (US Patent 6,732,221).

With respect to independent claims 1, 20, 32, and 34:

As per claims 1 and 34, Chang disclosed a method for wear leveling of a multi-block memory containing data, usable in multi-block memory activities, comprising the steps of:

detecting an at least one triggering signal (Fig. 3, item 304); and

copying or relocating the data of an at least one first memory block containing an at least one memory element of the multi-block memory to an at least one second

memory block of the multi-block memory after detecting the at least one triggering signal, wherein said at least one second memory block does not contain said data before said copying or relocating (Fig. 4, item 420, Fig. 6, item 612, and page 8, paragraph 0078, lines 1-7);

wherein said at least one second memory block does not contain said data before said copying or relocating is an inherent feature of Chang since "said data" does not existed in "the second block", otherwise it would be redundant and inefficient to copy or relocate "said data" from "the first block" to "the second block" in Chang.

As per claims 20 and 32, Chang disclosed a multi-block memory containing data, usable in multi-block memory activities (See Fig. 1b, item 11);

a memory pointer controller (Fig. 1a, item 128), responsive to the update signal (Fig. 1a, item 130, and Fig. 3, item 304), wherein interface 130 will inherently comprising data signaling to memory controller 128;

a memory wear controller (Fig. 1b, item 128), responsive to a triggering signal (Fig. 1a, item 130) or to a further triggering signal (Fig. 1b, item 15), for providing a data-relocation signal (Fig. 1b, item 17) to the multi-block memory (Fig. 1b, item 11) to relocate the data from an at least one first memory block containing an at least one memory element of the multi-block memory to an at least one second memory block of the multi-block memory(Fig. 4, item 420, Fig. 6, item 612, and page 8, paragraph 0078, lines 1-7);

wherein said at least one second memory block does not contain said data before said copying or relocating is an inherent feature of Chang since "said data" does

not existed in "the second block", otherwise it would be redundant and inefficient to copy or relocate "said data" from "the first block" to "the second block" in Chang.

As per claims 1, 20, 32, and 34, Chang did not explicitly teach wherein no information on a usage of said at least one first memory block, at least one second memory block or at least one memory element is provided for performing said copying or relocating.

However, Ban discloses a random process of a flash data manager to enhance the wear leveling of a flash memory. See col. 5, lines 29-39, wherein the method of moving memory content from one location to another is randomly assigned and there is no usage information provided for performing such memory allocation and relocation.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Chang with the method Ban in order to arrive at the current invention. The motivation of doing so is to provide a methodology for improving wear leveling for all units, including static units, in a Flash devices, with a substantially decrease in required system resources as taught by Ban at col. 6, lines 28-31.

With respect to claims 2, 3, 5-15, 19, 21-31, 33, and 35:

As per claims 2, 5, 28, and 29, Chang et al. disclosed a method, wherein each of the at least one first memory block and the at least one second memory block contains only one memory element (claims 2 and 28) or contains more than one memory element (claims 5 and 29). See paragraph 0008, wherein a block is generally a

storage element contain at least one memory page and a block will comprise only one page (one storage element) if the page size is equal to the block size;

wherein said at least one second memory block does not contain said data before said copying or relocating is an inherent feature of Chang since "said data" does not existed in "the second block", otherwise it would be redundant and inefficient to copy or relocate "said data" from "the first block" to "the second block" in Chang et al.

As per claims 3, 19, 23, 33, and 35, the method of updating a first memory pointer originally pointed to the at least one second memory block before said copying or relocating to point to the at least one first memory block after said copying or relocating is an inherent feature in Chang since updating a memory pointer to be pointed to a new data location after the data was moved is required in the computer art in order to avoid data being misallocated and taking up the unnecessary storage are.

As per claim 6, Chang disclosed a wherein the data of an at least one additional block of the multi-block memory is relocated to an at least one further additional block of the multi-block memory after detecting the at least one triggering signal. See Fig. 4, item 420, Fig. 6, item 612, and page 8, paragraph 0078, lines 1-7.

wherein said at least one second memory block does not contain said data before said copying or relocating is an inherent feature of Chang since "said data" does not existed in "the second block", otherwise it would be redundant and inefficient to copy or relocate "said data" from "the first block" to "the second block" in Chang.

As per claims 7 and 21, Chang disclosed a method, wherein said copying or relocating is performed according to predetermined criteria. See Fig. 4, wherein the copying is performing at a predetermined algorithm according to the flow chart.

As per claim 10, Chang disclosed a method, wherein said copying or relocating of the data occurs only after detecting a predetermined number of the at least one triggering signal. See Fig. 4, item 408, wherein the copying is occurred after determined that erase count is low compared to the average. The number of triggering signal is equivalent to the number of erasure triggered by the number of access request.

As per claim 11, Chang disclosed a method, wherein the at least one triggering signal corresponds to a read operation. See Fig. 3, item 306, wherein the obtaining after the initialization request is equivalent to the read operation.

As per claim 12, Chang disclosed a method, wherein the at least one triggering signal corresponds to a write operation. See Fig. 3, item 340, wherein storing is equivalent to write operation.

As per claim 13, a time clock pulse is an inherent feature in the computer art at the hardware level wherein the falling edge pulse or the rising edge clock pulse will trigger a predetermined operation which would have been programmed by those skilled

in the art in order to synchronize the all of the components and the operation of a computer to work together and maintaining the data and time.

As per claim 14, Chang disclosed a method, wherein the at least one triggering signal corresponds to the detection of a predetermined number of read/write operations or clock pulses. Claim 14 comprising the subject matters which already claimed in claims 11-13. Therefore, claim 14 is rejected under the same rationale as in combination of 11-13.

As per claim 15, Chang disclosed a method, wherein said copying or relocating of the data occurs a predetermined number of times between the triggering signals. See Fig. 4, wherein the triggering signal is equivalent to the number of triggering signals from the erasure trigger and the memory blocks are being relocated after a predetermined number of erasure counts.

As per claim 22, Chang disclosed an electronic device, wherein the memory pointer signal contains a physical address (Fig. 5a, mapping table 462 with physical block address) in the multi-block memory to be accessed for enabling an at least one further data relocation of the data located at the physical address and optionally an address of a first memory pointer. See Fig. 4, item 420, Fig. 6, item 612, and page 8, paragraph 0078.

As per claim 24, Chang disclosed an electronic device, wherein the memory wear controller and the memory pointer controller are implemented as a combination of software and hardware components. See paragraph 0048, lines 9-11 and paragraph 0056, lines 1-7, wherein the software is executed by microprocessor.

As per claim 25, Chang disclosed an electronic device, wherein the memory wear controller and the memory pointer controller are implemented as hardware. See page 4, paragraph 0049, lines last sentence, wherein the microprocessor as an hardware implemented to execute and control the memory control system.

As per claim 26, Chang disclosed an electronic device, wherein the hardware is implemented using a finite state machine. See page 5, paragraph 0051, lines 4-5, wherein the finite state machine is implemented in the memory control system.

As per claim 27, Chang disclosed an electronic device, wherein the memory wear controller and the memory pointer controller are implemented as software. See page 5, paragraph 0056, lines 4-6, wherein the software/code enable the memory to be addressed, read, or stored into.

As per claim 30, Chang disclosed an electronic device, wherein said copying or relocating of the data from the at least one first memory block and updating the location of the memory pointers are performed according to predetermined criteria. See Fig. 4,

wherein the copying is performing at a predetermined algorithm according to the flow chart.

As per claim 31, a triggering detector responsive to a triggering signal is an inherent feature in the computer art since signal triggering is required in order to enable the communication between the circuit components such as processor, memory, and memory controller.

3. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US Pub 2004/0177212) and Ban (US Patent 6,732,221) and further in view of Khalid et al. (US Pub 2003/0012661).

As per claim 17, Chang et al. and Ban did not explicitly disclose a method, wherein all the data contained in the multi-block memory is copied or relocated at the same time.

Khalid et al. discloses a method of writing the data into the memory block at the same time. See paragraph 0008, lines 2-7.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Change et al. and Ban with the method of Khalid et al. in order to arrive at the current invention since it will further benefit the wear leveling strategies of memory cells as taught by Khalid et al. on paragraph 0036, lines 1-4.

Response to Arguments

4. Applicant's arguments with respect to claims 1-15, 17-35 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendment.

With respect to Applicant's argument on page 14, last paragraph regarding claim 10. First of all, claim 10 is a depend claim instead of independent claim as stated by the Applicant. Secondly, claim 10 does not recite the limitation of "more than one trigger signal". Therefore, no response is necessary toward the argument set forth.

With respect to Applicant's argument on page 15, first paragraph regarding claim 13. The clock pulse as indicated by Examiner is not recited in Chang et al., however it is an inherent feature in Change et al. system. An inherent feature is not the same as a well known feature as being argued by the Applicant. An inherent feature is a feature that has to be exist within a system in order the system to operate or perform determined tasks or operations. See MPEP Paragraph 2112[R-3] for further clarification.

Allowable Subject Matter

5. Claims 4 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In respect to claim 4, Chang and relevant prior arts failed to disclose a method as disclosed in claim 4.

In respect to claim 18, Chang and relevant prior arts failed to disclose the memory addressing configuration as disclosed in claim 18.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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